2. BK2401/BK2421 and nRF24L01 What's the difference?

BK2401 and BK2421 The only difference is: BK2401 supports only the air data rate 1Mbps, 1Mbps and 2Mbps and BK2421 supports the air data rate. BK2401/BK2421 highly compatible with the nRF24L01, the biggest difference between the two is that the former two BANK registers (Bank0, Bank1), while the nRF24L01 only one, so BK2401/BK2421 need to power-on initialization Bank1. The following section includes the design point and the difference must be considered under normal circumstances without regard to the points of difference.

2.1 The design must take into account differences in point:

No.	Differences must be considered when the design points	nRF24L01	BK2401/BK2421	Remarks
1	RF front-end matching circuit	The same matching circuit, component values are different.	The same structure matching circuit, component values are different. Specific design see [2].	
2	Bank number register	1	2 (Bank0, Bank1)	Bank1 is to test and register extensions.
3	Power-on initialization	No	Need to initialize Bank1, follow these steps: (1) read status of the current Bank Bank0_REG7 [7] = RBANK = (0: Bank0; 1: Bank1), if Bank0, the use of SPI Bank ACTIVATE +0 x53 switch command to switch to Bank1; if Bank1, go to (2). (2) initialization Bank1 register Register values are as follows: 0xE2014B40, / / REG0 0x00004BC0, / / REG1 0x028CFCD0, / / REG2 0x41390099, / / REG3 0x0B869ED9, / / REG4 0xA67F0624, / / REG5 --- 0x00127300, / / REG12 0x36B48000, / / REG13 0x412008048120CFF7FEFFFF, / / REG14 Note: Bank1 the REG0 to REG8 write the following order: high byte first, then the low byte; each byte from the high and then low, the specific see [3]. Bank1's REG9 read and write to the REG14 and order and nRF24L01 Bank0 the same: first the low byte,	

			then high byte; each byte is still from high to low. (3) SPI Bank ACTIVATE +0 x53 switch command to switch to Bank0.	
4	Address selection Address bytes 3 ~ 5bytes, if dissatisfied with 5bytes need to fill five bytes. Address bytes 3 ~ 5bytes, if dissatisfied with 5bytes, need to fill in any unused high byte address to fill the 5 bytes.	Address selection Address bytes 3 ~ 5bytes, if dissatisfied with 5bytes need to fill five bytes. Address bytes 3 ~ 5bytes, if dissatisfied with 5bytes, need to fill in any unused high byte address to fill the 5 bytes.	Address selection Address bytes 3 ~ 5bytes, if dissatisfied with 5bytes need to fill five bytes. Address bytes 3 ~ 5bytes, if dissatisfied with 5bytes, need to fill in any unused high byte address to fill the 5 bytes.	

2.2 The design point of difference is usually no need to consider:

No.	Usually not considered in the design point of difference	nRF24L01	BK2401/BK2421	Remarks
1	CSN timing requirements	CSN is not required in the finished later than the data pulled CLK operation.	CSN write data in the low state after the CLK and then pulled up at least half must be later than the time of CLK, and the CSN is not greater than the rise time 100ns.	
2	CE is set low after, RX_DR interrupt cleared	CE is set low after the break will not be cleared.	When CE is set low after, RX_DR break automatically cleared, so set the CE low before treatment interruption.	
3	PTX, PRX interrupt time	When PRX sent with the ACK PAYLOAD end when PRX: TX_DS a packet delay than RX_DR set 1; PTX-side: RX_DR and TX_DS also set to 1.	When PRX sent with the ACK PAYLOAD end when PRX: RX_DR and TX_DS also set 1; PTX-side: TX_DS first set 1; RX_DR delayed 2-3us than TX_DS set to 1.	If the ACK with PAYLOAD need attention.

4	PTX equipment to receive FIFO overflow treatment	If the RX FIFO has received over three levels, you receive the package will not overwrite the data in the FIFO, the interrupt will trigger RX_DR.	If the RX FIFO has received over three levels, you receive the package will not overwrite the data in the FIFO, and will not trigger RX_DR interrupt.	If the ACK with PAYLOAD need attention.
5	CD detection	There is no control switch, you can not set threshold, and threshold value varies with temperature ± 5dB, CD will automatically be cleared from time to time.	A control switch, a comparison threshold, Bank1_REG5 [29:26] To compare the threshold 0:-97dBm, 15:-67dBm, step of 2dB. When the detected interference signal is greater than the continuous 128us set threshold, Bank0_REG9 [0] will be set to 1, and will always remain one until after the value of reading CD automatically cleared. If no CD, turn off the CD to save power (1mA or so, the default initial value is off).	BK2421 improve RSSI detection accuracy.
6	REUSE_TX_PL command	When replacing the channel, or the CE low, or switch TX / RX mode, REUSE command is still valid.	When replacing the channel, or the CE low, or switch TX / RX mode, the command will automatically end. If you need to start again REUSE, you need to resend the command.	If you use the REUSE command should pay attention.
7.	Bank0_REG6 [4] = RF_PWR	PLL_LOCK, forcibly closed nRF24L01 launch, launch-carrier complex procedures.	Do not have this bit, single-carrier transmitter to control the Bank1, Bank1_REG4 = 0xD99E8621	Simple single-carrier launch, just write a register to Bank1.

8.	Transmit power	Maximum 0dBm, four control.	Can control the output power of eight, maximum 5dBm, a minimum of-40dBm, the specific power levels, see the back of the "other common problems."	Transmit power can provide more choices.